

**IN THE CLAIMS**

The following claim listing is intended to reflect amendment of previously pending claims 33, 39, 55, 61-62, 67, 72-74, 78-79, 82-83, and 86. Claims 33-40 and 55-86 remain pending in the present application.

The specific amendments to individual claims are detailed below.

1. - 32. (Canceled)

33. (Currently Amended) A logic ~~device~~ circuit and a memory ~~device~~ circuit structure on a single substrate, comprising:

a first transistor having a source and a drain region in the substrate separated by a channel region in the substrate, wherein the first transistor includes a dielectric layer of a first thickness, including a top layer which exhibits ~~a high~~ higher resistance to oxidation ~~at high temperatures~~ than the substrate material, separating a gate from the channel region; and

a second transistor having a source and a drain region in the substrate separated by a channel region in the substrate, wherein the second transistor includes a dielectric layer of second thickness different from the first thickness, separating a gate from the channel region.

34. (Original) The structure of claim 33, wherein the first transistor is a transistor for the logic device and the second transistor is a transistor for the memory device.

35. (Original) The structure of claim 33, wherein the first transistor having a dielectric layer of a first thickness includes a dielectric layer having a thickness of less than 7 nanometers.

36. (Original) The structure of claim 33, wherein the first transistor having a dielectric layer of a first thickness includes a bottom layer of silicon dioxide (SiO<sub>2</sub>) and a top layer of silicon nitride (Si<sub>3</sub>N<sub>4</sub>).

37. (Original) The structure of claim 33, wherein the second transistor having a dielectric layer of second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO<sub>2</sub>).

38. (Original) The structure of claim 33, wherein the second transistor having a dielectric layer of second thickness includes a dielectric layer having a thickness of less than 12 nanometers.

39. (Currently Amended) The structure of claim 33, wherein the first transistor which includes a dielectric layer of a first thickness and having a top layer ~~which exhibits a high resistance to oxidation at high temperatures~~ includes a top layer of silicon nitride (Si<sub>3</sub>N<sub>4</sub>) which comprises approximately a third of the first thickness of the dielectric layer.

40. (Original) The structure of claim 33, wherein the first transistor which includes a dielectric layer of a first thickness includes a dielectric layer having a thickness of less than 7 nanometers, wherein the dielectric layer has a bottom layer of silicon dioxide (SiO<sub>2</sub>), and wherein the top layer is silicon nitride (Si<sub>3</sub>N<sub>4</sub>).

41. - 54. (Canceled)

55. (Currently Amended) A logic ~~device~~ circuit and a memory ~~device~~ circuit structure on a single substrate, comprising:

a first transistor, wherein the first transistor includes:

a first dielectric layer of a first thickness less than 5 nanometers (nm);

a top layer which exhibits ~~a high~~ higher resistance to oxidation ~~at high temperatures than the substrate material~~; and

a second transistor, wherein the second transistor includes a second dielectric layer of a second thickness different from the first thickness.

56. (Previously Presented) The structure of claim 55, wherein the first dielectric layer and the top layer together have a thickness of less than 7 nanometers (nm).

57. (Previously Presented) The structure of claim 55, wherein first dielectric layer of a first thickness includes silicon dioxide (SiO<sub>2</sub>) and the top layer includes silicon nitride (Si<sub>3</sub>N<sub>4</sub>).
58. (Previously Presented) The structure of claim 55, wherein the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO<sub>2</sub>).
59. (Previously Presented) The structure of claim 55, wherein the second dielectric layer of a second thickness includes a dielectric layer having a thickness of less than 12 nanometers.
60. (Previously Presented) The structure of claim 55, wherein the top layer includes a top layer of silicon nitride (Si<sub>3</sub>N<sub>4</sub>) which comprises approximately a third of the first thickness of the first dielectric layer.
61. (Currently Amended) The structure of claim 55, wherein the top layer exhibits a ~~high~~ higher resistance to boron penetration ~~at high temperatures~~ than the substrate material.
62. (Currently Amended) A logic ~~device circuit~~ and a memory ~~device circuit~~ structure on a single substrate, comprising:
- a first transistor, wherein the first transistor includes:
    - a first dielectric layer of a first thickness less than 5 nanometers (nm);
    - a top layer which exhibits a ~~high~~ higher resistance to boron penetration ~~at high temperatures~~ than the substrate material; and
  - a second transistor, wherein the second transistor includes a second dielectric layer of a second thickness different from the first thickness.
63. (Previously Presented) The structure of claim 62, wherein the first dielectric layer and the top layer together have a thickness of less than 7 nanometers (nm).

64. (Previously Presented) The structure of claim 62, wherein first dielectric layer of a first thickness includes silicon dioxide (SiO<sub>2</sub>) and the top layer includes silicon nitride (Si<sub>3</sub>N<sub>4</sub>).

65. (Previously Presented) The structure of claim 62, wherein the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO<sub>2</sub>).

66. (Previously Presented) The structure of claim 62, wherein the second dielectric layer of a second thickness includes a dielectric layer having a thickness of less than 12 nanometers.

67. (Currently Amended) A logic ~~device~~ circuit and a memory ~~device~~ circuit structure on a single substrate, comprising:

a first transistor, wherein the first transistor includes:

a first dielectric layer of a first thickness less than 5 nanometers (nm);

a silicon nitride (Si<sub>3</sub>N<sub>4</sub>) top layer which exhibits a ~~high~~ higher resistance to oxidation ~~at high temperatures than the substrate material~~; and

a second transistor, wherein the second transistor includes a second dielectric layer of a second thickness different from the first thickness.

68. (Previously Presented) The structure of claim 67, wherein the first dielectric layer and the top layer together have a thickness of less than 7 nanometers (nm).

69. (Previously Presented) The structure of claim 67, wherein the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO<sub>2</sub>).

70. (Previously Presented) The structure of claim 67, wherein the second dielectric layer of a second thickness includes a dielectric layer having a thickness of less than 12 nanometers.

71. (Previously Presented) The structure of claim 67, wherein the silicon nitride (Si<sub>3</sub>N<sub>4</sub>) top layer includes a silicon nitride (Si<sub>3</sub>N<sub>4</sub>) top layer with a thickness of approximately a third of the first thickness of the first dielectric layer.

72. (Currently Amended) The structure of claim 67, wherein the top layer exhibits a ~~high~~ higher resistance to boron penetration ~~at high temperatures~~ than the substrate material.

73. (Currently Amended) A logic ~~device circuit~~ and a memory ~~device circuit~~ structure on a single substrate, comprising:

a first transistor, wherein the first transistor includes:

a first dielectric layer of a first thickness less than 5 nanometers (nm);

a top layer of approximately a third of the first thickness, which exhibits a ~~high~~ higher resistance oxidation ~~at high temperatures~~ than the substrate material; and

a second transistor, wherein the second transistor includes a second dielectric layer of a second thickness different from the first thickness.

74. (Currently Amended) The structure of claim 73, wherein the top layer exhibits a ~~high~~ higher resistance to boron penetration ~~at high temperatures~~ than the substrate material.

75. (Previously Presented) The structure of claim 73, wherein the first dielectric layer and the top layer together have a thickness of less than 7 nanometers (nm).

76. (Previously Presented) The structure of claim 73, wherein the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO<sub>2</sub>).

77. (Previously Presented) The structure of claim 73, wherein the second dielectric layer of a second thickness includes a dielectric layer having a thickness of less than 12 nanometers.

78. (Currently Amended) A logic ~~device circuit~~ and a memory ~~device circuit~~ structure on a single substrate, comprising:

a first transistor, wherein the first transistor includes:

a first dielectric layer of a first thickness less than 5 nanometers (nm);

a top layer which exhibits a ~~high~~ higher resistance to oxidation ~~at high~~

~~temperatures than the substrate material~~; and

a second transistor, wherein the second transistor includes a second dielectric layer of a second thickness different from the first thickness, wherein the second thickness is less than 12 nanometers (nm).

79. (Currently Amended) The structure of claim 78, wherein the top layer exhibits a ~~high~~ higher resistance to boron penetration ~~at high temperatures~~ than the substrate material.

80. (Previously Presented) The structure of claim 78, wherein the first dielectric layer and the top layer together have a thickness of less than 7 nanometers (nm).

81. (Previously Presented) The structure of claim 78, wherein the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO<sub>2</sub>).

82. (Currently Amended) A logic ~~device circuit~~ and a memory ~~device circuit~~ structure on a single substrate, comprising:

a first transistor, wherein the first transistor includes:

a first dielectric layer of a first thickness less than 5 nanometers (nm);

a silicon nitride (Si<sub>3</sub>N<sub>4</sub>) top layer of approximately a third of the first thickness, which exhibits a ~~high~~ higher resistance to oxidation ~~at high temperatures~~ than the substrate material; and

a second transistor, wherein the second transistor includes a second dielectric layer of a second thickness different from the first thickness, wherein the second thickness is less than 12 nanometers (nm).

83. (Currently Amended) The structure of claim 82, wherein the top layer exhibits a ~~high~~ higher resistance to boron penetration ~~at high temperatures~~ than the substrate material.

84. (Previously Presented) The structure of claim 82, wherein the first dielectric layer and the top layer together have a thickness of less than 7 nanometers (nm).

85. (Previously Presented) The structure of claim 82, wherein the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO<sub>2</sub>).

86. (Currently Amended) A logic ~~device~~ circuit and a memory ~~device~~ circuit structure on a single substrate formed by the method comprising:

forming a pair of transistor channel regions on the single substrate;

forming a pair of gate oxides to a first thickness on the pair of channel regions;

wherein forming the pair of gate oxides to a first thickness includes forming the pair of gate oxides to a thickness of less than 5 nanometers (nm) by krypton plasma generated atomic oxygen ~~at approximately 400 degrees Celsius;~~

forming a ~~thin~~ dielectric layer on one of the pair of gate oxides, wherein the ~~thin~~ dielectric layer exhibits higher resistance to oxidation at high temperatures than the substrate material; and forming the other of the pair of gate oxides to a second thickness different from the first thickness.

PRELIMINARY AMENDMENT

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